Amendments to the Claims

1. (Currently Amended): A computer-implemented method for designing circuits~~of optimizing a circuit design model during logic synthesis~~, comprising:

during a logical synthesis stage of a circuit design,

generating a network graph from a logical representation of the circuit design;

determining~~creating~~ a structural metric from a property of the network graph~~prior to physical design~~, wherein the structural metric predicts congestion characteristics during optimization of the circuit design~~being proportional routability of the circuit design model after the physical design~~; and

using the structural metric during the logic synthesis stage to optimize ~~create an optimized~~ the circuit design ~~model~~;

2. (Currently Amended): The method of claim 1, wherein using the structural metric during the logic synthesis stage ~~to create an optimized circuit design model~~ to optimize the circuit design comprises adding, deleting or substituting one or more circuits using a combination of boolean, algebraic and electrical optimizations ~~to create an optimized circuit design model~~.

3. (Currently Amended): The method of claim 1, wherein ~~creating a structural metric prior to physical design, the structural metric being proportional to the routability of the circuit design model after the physical design comprises creating a structural metric prior to physical design,~~ the structural metric ~~when applied to a graph of the circuit design model is directly proportional to a~~includes a measure of routing congestion of the circuit design ~~model~~ after placement and routing, the routing congestion being measured by an average and a peak number of wires crossing any bisection of the placed and routed circuit design ~~model~~.

4. (Currently Amended): The method of claim 1, wherein using the structural metric during the logic synthesis stage to optimize the circuit design comprises using the

structural metric during a technology independent synthesis stage of the logic synthesis stage.

5. (Currently Amended): The method of claim 1, wherein using the structural metric during the logic synthesis stage to optimize the circuit design comprises using the structural metric during a technology mapping stage of the logic synthesis stage.

6. (Currently Amended): The method of claim 1, wherein using the structural metric during the logic synthesis stage to optimize the circuit design comprises using the structural metric during a buffering stage of the logic synthesis stage.

7. (Currently Amended): The method of claim 1, further comprising incrementally updating the structural metric when logic changes are made to the circuit design ~~model~~.

8. (Currently Amended): The method of claim 7, wherein incrementally updating the structural metric when logic changes are made to the circuit design ~~model~~ comprises performing recomputation on circuits involved in an optimization and circuits affected by the optimization to provide a structural metric cost.

9. (Currently Amended): The method as in claim 7, wherein incrementally updating the structural metric when logic changes are made to the circuit design ~~model~~ comprises maintaining information regarding circuits affected by an optimization, which are computed when recomputation of the structural metric is necessary.

10. (Currently Amended): The method of claim 1, wherein ~~creating~~ the structural metric comprises ~~creating~~ any one of a distance metric, a sum-of-all-pairs-min-cut ("SAPMC"), and an expansion metric.

11. (Currently Amended): The method of claim 1, wherein ~~creating~~determining a structural metric comprises:

generating one or more possible optimizations;

incrementally updating the structural metric when the optimizations are made to the circuit design ~~model~~ to evaluate the cost of applying each of the one or more possible optimizations to the circuit design ~~model~~, the structural metric comprising any one of a distance metric, a sum-of-all-pairs-min-cut ("SAPMC"), and an expansion metric;

evaluating a structural metric cost of each of the one or more possible optimizations as given by the structural metric;

selecting an optimization from the one or more possible optimizations with the lowest structural metric cost; and

applying the optimization to the circuit design ~~model~~.

12. (Original): The method of claim 11, wherein generating the one or more possible optimizations comprises:

generating a structure-driven kernel factoring;

generating a structure-driven decomposition;

generating a structure-driven tech mapping; and

generating a structure-aware buffering.

13. (Currently Amended): A machine-readable medium having instructions stored thereon for optimizing a circuit design model during logic synthesis, comprising the steps of:

during a logical synthesis stage of a circuit design,

generating a network graph from a logical representation of the circuit design;

determining~~creating~~ a structural metric ~~prior to physical design~~ from a property of the network graph, wherein the structural metric ~~being proportional to a~~ predicts congestion characteristics during optimization ~~routability of~~ the circuit design ~~model after the physical design~~; and

using the structural metric during logic synthesis to optimize~~create an optimized~~ the circuit design ~~model~~.

14. (Currently Amended): A system for designing circuits~~optimizing a circuit design model during logic synthesis~~, comprising:

means for creating a structural metric from a property of a network graph during a logical synthesis stage of a circuit design~~prior to physical design~~, wherein the network graph is derived from a logical representation of the circuit design and the structural metric predicts congestion characteristics during optimization ~~being proportional to a routability~~ of the circuit design ~~model after the physical design~~; and

means for using the structural metric during the logic synthesis stage to optimize~~create an optimized~~ the circuit design ~~model~~.